REMARKS

Summarizing the Office Action dated August 21, 2003, the Examiner rejects claims 1-4, 11-14, 17-21, 24 and 25 under 35 U.S.C. §103(a) as obvious over Murakami 6,181,098 in view of Rhee et al. 6,147,561. He rejects claims 8, 16, 23 and 26 as obvious over Murakami and Rhee as applied to claims 1, 4, 11, 12, 17 and 24 and in further view of Trachtenberg 6,121,747. Claim 10 stands rejected as obvious over Murakami and Rhee as applied to claim 1 and in further view of Lundberg et al. 5,811,998. Claim 15 stands rejected as obvious over Murakami and Rhee as applied to claims 11 and 12 and in further view of Rogers 5,371,425. Claim 28 stands rejected as obvious over Murakami in view of Tanaka 5,452,326. The Examiner also objects to various limitations of claims 9 and 26 for not reciting a proper antecedent basis. The Applicant notes with thanks the Examiner's indication of allowable subject matter in claims 5-7, 9 and, if rewritten in independent form to include the limitations of the base and any intervening claims, claims 22 and 27.

By this response, the Applicant hereby amends claims 9, 17, 24 and 26 and adds new claims 29-32. Claims 18 and 25 have been canceled while claims 1-8, 10-16, 19-23, 27 and 28 remain as originally presented. As for the originally presented claims, the Applicant respectfully requests reconsideration.

As a preliminary matter, however, the Applicant's newly presented claims 29, 30 and 31 merely embody the subject matter of original claims 22, 27 and claim 9, respectively, rewritten as independent claims. The Applicant submits these claims are allowable because the prior art does not anticipate nor render them obvious and the Examiner has indicated their allowability. Further, claims 17 and 24 now contain the subject matter of claims 18 and 25, respectively, thereby the Applicant has canceled 18 and 25. Claims 9 and 26 have minor amendments in accordance with the Examiner's suggestion to provide a proper antecedent basis for various limitations thereof. Claim 32 embodies the subject

matter of claim 1 except for the limitation regarding modeling non-linear components of the reference signal.

Turning now to the substance of the rejections, Murakami generally teaches:

> an improved DC motor control circuit that is constructed from a hardware circuit to supplement or assist the software control operations by the CPU and that is capable of stopping the DC motor at a fixed position, while increasing the processing capability of the CPU by reducing the number of interrupt routines required to be executed by the CPU. *Col. 3, ll. 22-29.*

Specifically, Murakami teaches an ink jet printer 100 having a DC motor 8 for the reciprocating driving of a print head 6. An encoder sensor 90 measures movement of a carriage 62 thereby "measuring the rotation of the DC motor 8." *Col. 3, l. 37.* A position detection signal output circuit 9 supplies signals output from the encoder sensor 90 to a DC motor control circuit 7 that exists electrically separate from the CPU 1 via an I/O port 5. Based upon these signals, the DC motor control circuit 7 then:

> determines the direction in which the print head is actually moving. The DC motor control circuit 7 then increments or decrements its internal counter based on the determined direction, thereby producing a position count value 105 indicative of the present position of the print head 6.
>
> The DC motor control circuit 7 also judges whether or not the print head reaches one of a pair of predetermined stop positions (described later). When the DC motor control circuit 7 determines that the print head reaches one of the predetermined stop positions, the DC motor control circuit 7 performs a stop control operation onto the control circuit 50 to immediately stop the print head 6 at the predetermined stop position without relying on the CPU 1. *Col. 11, ll. 19-33.*

To accomplish the foregoing, the DC motor control circuit 7 includes a plurality of processing circuits, including a position detection signal processing

circuit 101, a position count processing circuit 104, a stop control circuit 20 and a stop detection circuit 30.

Rhee et al. teaches a phase lock loop (PLL) with traditional elements including a phase frequency detector (PFD) 14, a low pass filter 20, a VCO 22 and feedback loop such that the PFD compares a feedback signal to a reference signal. In addition, a plurality of time delay elements 200, 202 exist in the PLL such that the PFD also compares time delayed versions 206', 206", 206'" of the reference signal 206 with correspondingly time delayed versions 208', 208", 208'" of the feedback signal 208. Purportedly, such enhances the gain of the PLL circuit.

In his rejection, the Examiner submits that Rhee teaches that "the output of the phase detector follows a non-linear function (fig. 2, based on time delay elements #'s 200)." *P. 3, ll. 10-11, Office Action 8-21-03.* Thereafter, he relies on this characterization, in combination with Murakami, to reject claim 1 (and others) as obvious.

The Applicant, however, respectfully contends that such does not accurately reflect the teaching of Rhee nor does it serve as a proper basis in rendering any of the claims obvious. Moreover, the Applicant finds no other instances of a characterization or position of the prior art references regarding the Applicant's claim limitations directed toward "non-linear components" or "a describing function" and concludes the Examiner's only position regarding the rejection of claims containing these limitations is wholly founded on the above-quoted Rhee characterization.

As the Examiner will recall, claim 1, for example, recites the following:

1. A control system for controlling movement of a DC motor, comprising

a movement detector to detect movement of a DC motor and output a corresponding feedback signal;

a digital phase detector to compare phase of the feedback signal from said

movement detector with phase of a reference signal and output a comparison signal, ***wherein the digital phase detector follows a describing function to model non-linear components of the reference signal***; and

a digital loop filter to filter noise from the comparison signal for control of the DC motor.

As highlighted in bold-italics, the claim recites that the digital phase detector "follows a describing function" and does so "to model non-linear components" of a reference signal that the digital phase detector compares a phase thereof to a phase of a feedback signal. It does not, however, recite that the digital phase detector has an "output" that follows a non-linear function as the Examiner argues that Rhee does.

As the Examiner will notice, claim 1 does recite an output of the phase detector and refers to such as "a comparison signal." Yet, the comparison signal relates in no manner to the digital phase detector's "follow[ing] a describing function to model non-linear components of the reference signal." Still further, the non-linearity recited in the claims expressly relates to "components of the reference signal" and not to an output of a digital phase detector.

As for the Examiner's assertion that Rhee teaches an "output" of the phase detector that follows a non-linear function "based upon time delay elements #'s 200," the Applicant submits that the Rhee time delay elements 200, 202 merely serve to shift a given input signal in the time domain, by some delay period T. In this manner, a circuit achieves a signal output from the time delay element with the same exact waveform as the input signal, but only with a different phase. In other words, time delayed signals exactly represent a given input signal except for being later in time. They do not, however, implicate the linearity or non-linearity of the input signal let alone to cause "the output of the phase detector [to] follow[] a non-linear function" as the Examiner states.

Moreover, even if the Examiner's position that the time delay elements somehow enable a non-linear function, the Applicant stresses that Rhee's time delay elements appear on the front-side of the PFD 14 as inputs and are irrelevant to the "output of the phase detector" and to its following a "non-linear function" as contended.

Lastly, the Applicant asserts that nowhere does Rhee or Murakami alone or in combination expressly or inherently mention a describing function of a PFD 14 or DC motor control circuit 7, respectively, or that a reference input signal has non-linear components such that "a digital phase detector follows a describing function to model" such components as does pending claim 1. Accordingly, the Applicant respectfully requests consideration of the patentability of claim 1 in view of the combination of Murakami and Rhee.

Since claims 11, 17, 24 and 32 all have comparable limitations to claim 1, the Applicant incorporates the above arguments when requesting reconsideration. The specific claim limitations that support this position include "wherein the digital phase detector models non-linear components of the reference signal" (claim 11); "wherein said digital phase frequency detector follows a describing function" (claim 17); "said comparing step following a describing function" (claim 24); and "wherein the digital phase detector follows a describing function" (claim 32).

By their direct or indirect dependence upon claims 1, 11, 17 or 24, the Applicant also requests reconsideration of claims 2-10, 12-16, 19-23, 26 and 27.

Regarding the specific rejection to claim 10, the Applicant respectfully submits that the combination of Rhee and Lundberg is improper. Particularly, Rhee teaches time delay elements 200, 202 in a PLL for time-shifting inputs of the PFD 14. Conversely, Lundberg expressly teaches away from PLL's using delay elements. For example, at *col. 1, l. 49 et seq.*, Lundberg teaches:

[d]elay lock loops are also capable of achieving the desired

> synchronization by control of delay in a delay line. But delay lock loops also have attendant drawbacks and risks. If the delay line uses an analog control voltage, it is subject to the same problems mentioned above for conventional phase lock loops. If the delay line uses digital delay, then there is a penalty of clock phase contraction incurred when the delay lock loop must decrement.

Further, Lundberg then asserts that the prior art desires to "eliminate the risk, performance, penalties and cost associated with synchronization by conventional techniques." *Col. 1, ll. 58-60.* As the law provides, a reference that teaches away cannot serve to create a *prima facie* case of obviousness.[1]

The last rejection that requires addressing is that of claim 28. The Examiner's position is that the combination of Murakami and Tanaka render the claim obvious. According to the Office Action, Murakami "does not disclose modeling the phase detector in a closed loop, phase locked loop configuration with a describing function; and dampening the frequency response of the describing function by anticipating a step response of the motor during initial movement." *Page 6, lines 13-16, Office Action 8-21-03.* The Applicant agrees. Murakami shows none of these features.

The Examiner then looks to Tanaka, in combination with Murakami, as rendering the claim obvious. Specifically, "Tanaka discloses a digital phase locked loop circuit that provides damping features as cited above." *Id. at lines 17-18.* Thereafter, he concludes "it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the system of Murakami so the circuit is configured to carry out phase locked loop operations and dampen the frequency response as cited above, thereby providing the advantage of improving system excess response, as taught by Tanaka." *Page 6, line21 – Page 7, line 2, Office Action 8-21-03.*

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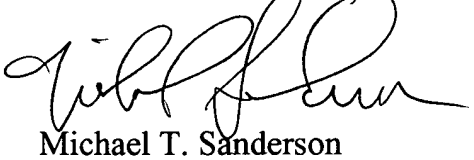
[1] *In re Gurley*, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994); *See United States v. Adams*, 383 U.S. 39 (1966); *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 USPQ 303 (Fed. Cir. 1983); Manual of Patent Examining Procedure §2141.02.

Nowhere, however, does the Examiner point out where Tanaka fills the void created by Murakami's lack of teaching of the "describing function." Moreover, Tanaka just does not inherently or expressly disclose a describing function let alone "modeling the phase detector in a closed loop, phase locked loop configuration with a describing function" as the claim requires. Thus, the Applicant respectfully submits these two references cannot render claim 28 as obvious in view thereof and the Examiner has provided no evidence to the contrary. Reconsideration is respectfully requested.

As a result, the Applicant submits that all pending claims are in a condition for allowance. If any matters require further attention, however, the Applicant requests the Examiner to contact the Applicant's attorney at the telephone number listed below in order to expedite the prosecution of this patent application. If any fees are due related to this response, the undersigned authorizes the deduction thereof from deposit account no. 11-0978.

Respectfully submitted,

KING & SCHICKLI, PLLC



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on November 20, 2003

Date 11-20-03 Carolina Perdomo